ABSTRACT

A packet analyzer for controlling a packet switch is segmented into a sequentially scanned array of packet analyzers, each of which is associated with a respectively different configuration function. When a packet is presented to the switch, a prescribed portion of the packet is sequentially coupled to the analyzers. As each analyzer examines the packet, it returns an indicator (e.g., '1' or '0') in accordance with whether the packet is associated with the configuration function of that analyzer. Once an analyzer indicates that it will accept the packet, the packet is forwarded to a stack associated with one or more virtual circuit ports embraced by that analyzer's configuration function, so that the packet may be forwarded to the appropriate virtual circuit output port, for transport over the network to a destination address. If the packet is not accepted by any analyzer prior to reaching the last analyzer of the array, the last analyzer will accept and destroy the packet to prevent memory overflow.